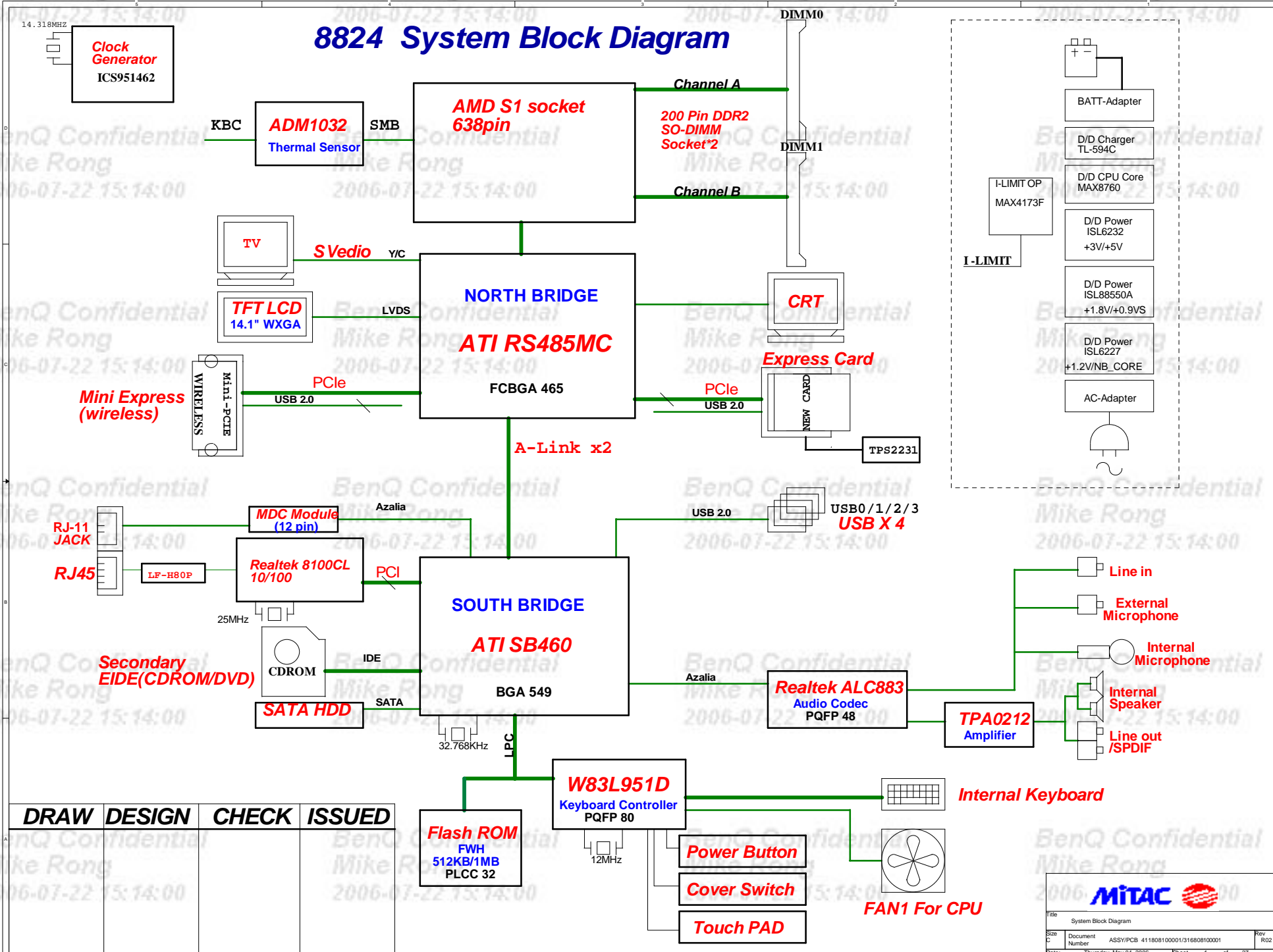


8824 System Block Diagram



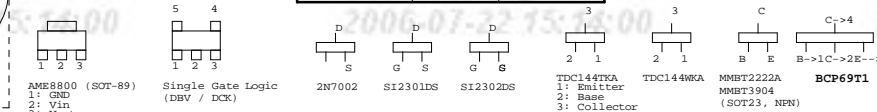
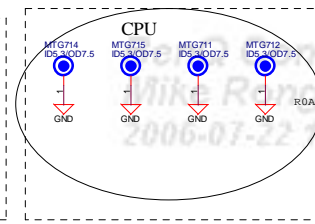
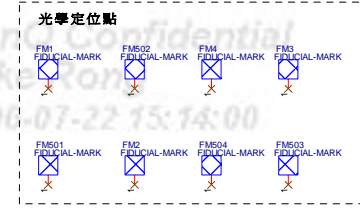
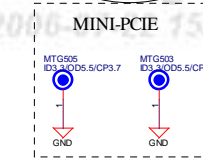
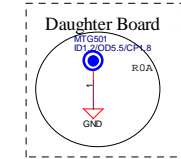
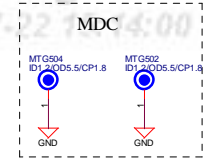
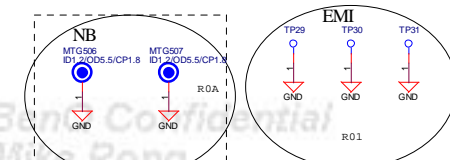
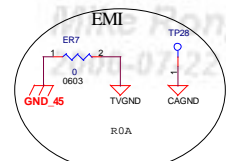
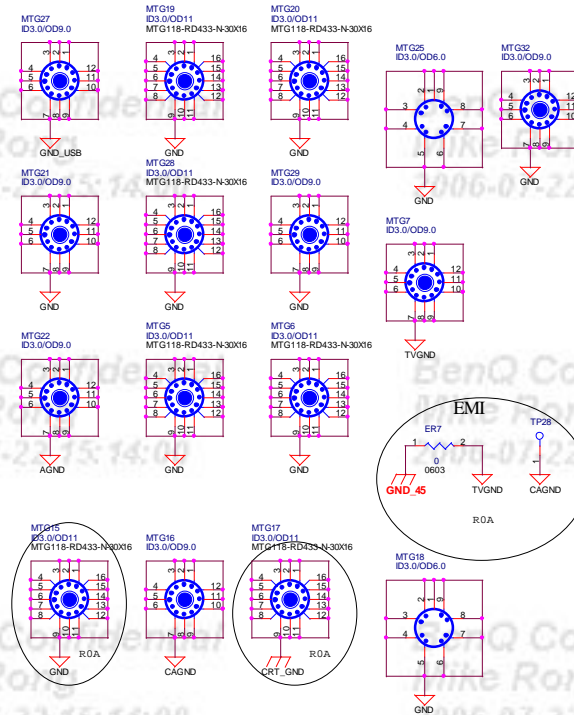
DRAW	DESIGN	CHECK	ISSUED

8824 R01

PROJECT CODE- G285
PRODUCT CODE- 8081

PCB P/N:31680810001
ASSY P/N:41180810001

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POWER STATES

STATE SIGNAL	VOTAGE	POWER ON	STR (S3)	STD (S4)	MEC-OFF (S5)	REMARK
SUSB#	-	HIGH	LOW	LOW	LOW	
SUSC#	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	0	0	0	0	
BATTERY	+12V	0	0	0	0	
VDD5	+5V	0	0	0	0	
VDD3	+3.3V	0	0	0	0	
VDD3S	+3.3V	0	0	0	0	ACC-IN X
+5V	+5V	0	0	X		X
+3V	+3.3V	0	0	X		X
+2.5V	+2.5V	0	0	X		X
+1.5V	+1.5V	0	0	X		X
+1.8V	+1.8V	0	0	X		X
+0.9VREF	+0.9V	0	0	X		X
+0.9V	+0.9V	0	0	X		X
+5VS	+5V	0	X	X		X
+3VS	+3.3V	0	X	X		X
+1.5VS	+1.5V	0	X	X		X
+1.8VS	+1.8V	0	X	X		X
+1.2VLDT_NB	+1.2V	0	X	X		X
NB_CORE	+1.2V	0	X	X		X
+CPU_CORE	+1.075~+1.100V	0	X	X		X

IDSEL

IDSEL	CHIP
AD20	RTL8100CL

PCIE LANE

LANE	DEVICE
1	Mini Card
2	Express Card

USB

PORT	DEVICE
5	Mini Card
6	Express Card

BUS MASTER

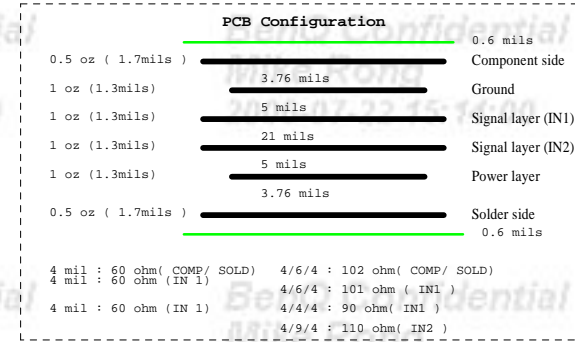
REQ/GNT	CHIP
-REQ1 / -GNT1	RTL8100CL

PCIINT

PCIINT	CHIP
INTB#	RTL8100CL

I2C / SMB Address

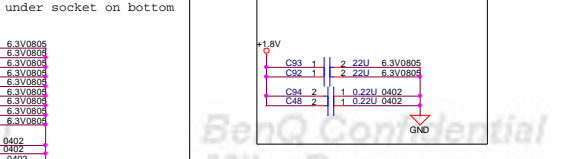
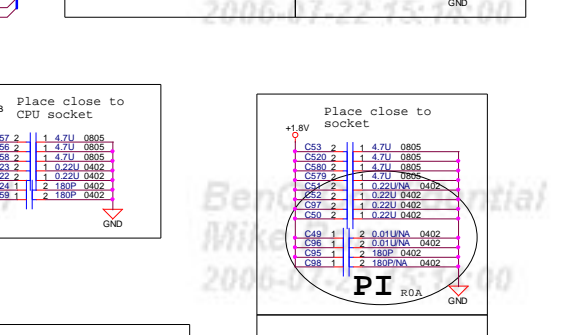
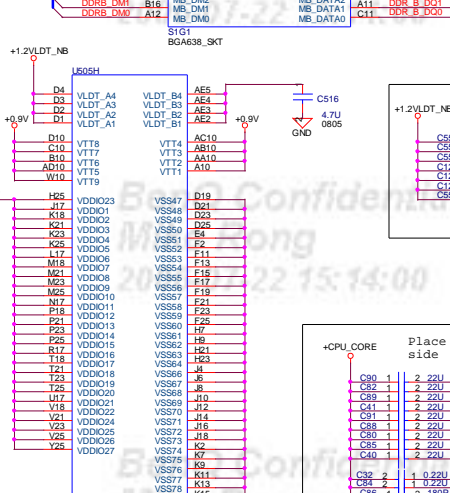
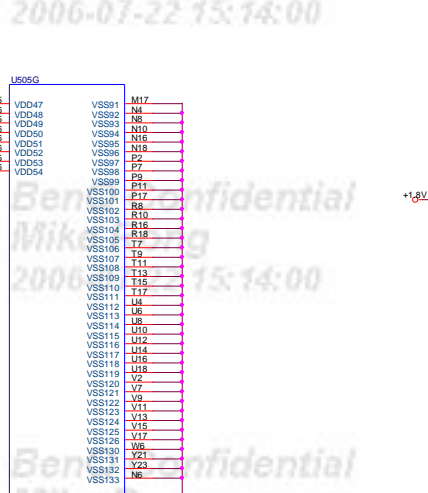
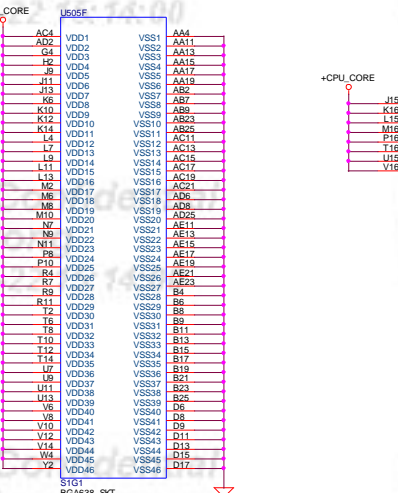
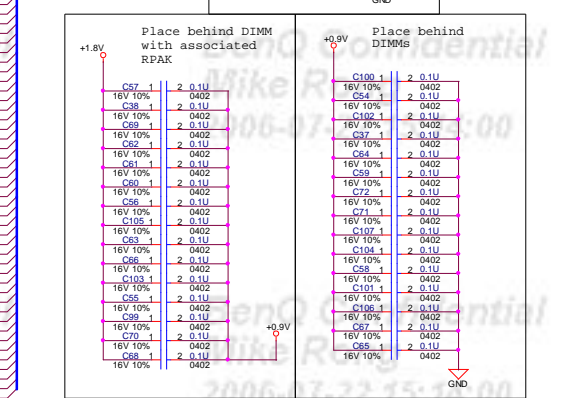
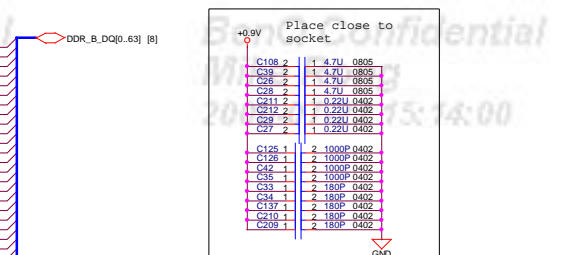
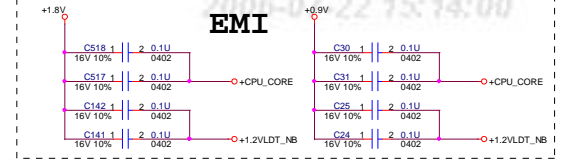
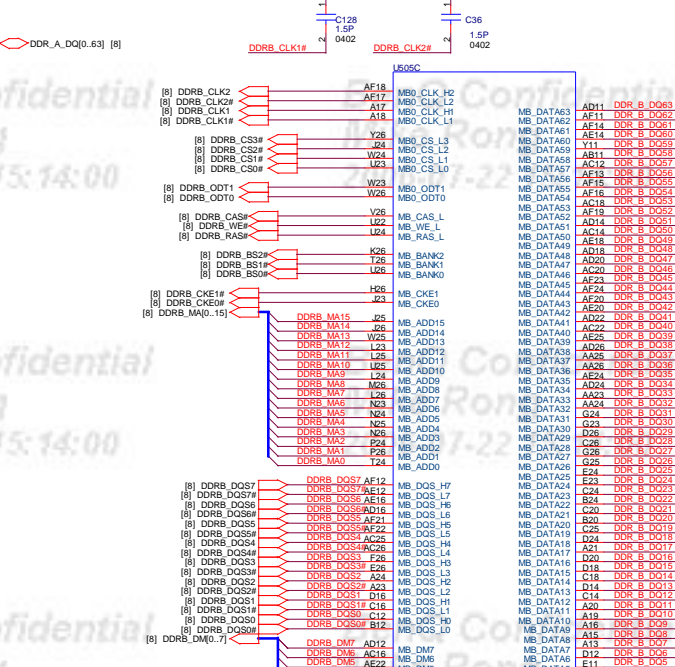
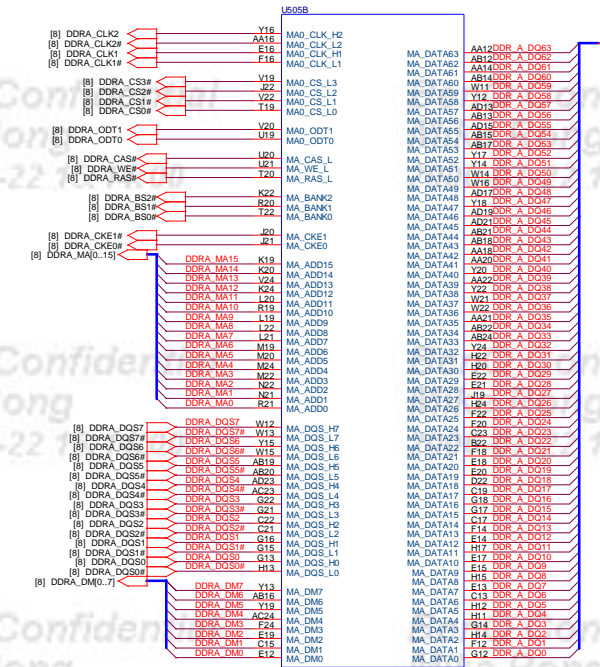
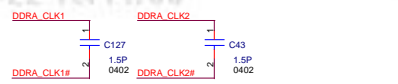
DEVICE	WRITE	READ
CLK GEN	D2	D3
DIMM0	A0	A1
DIMM1	A2	A3
LM86	98	99
LM89-1	9A	9B



MITAC

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Size: C
Document Number: ASSY/PCB 41180810001/31680810001
Rev: R02
Date: Thursday, May 04, 2006 Sheet: 2 of 27

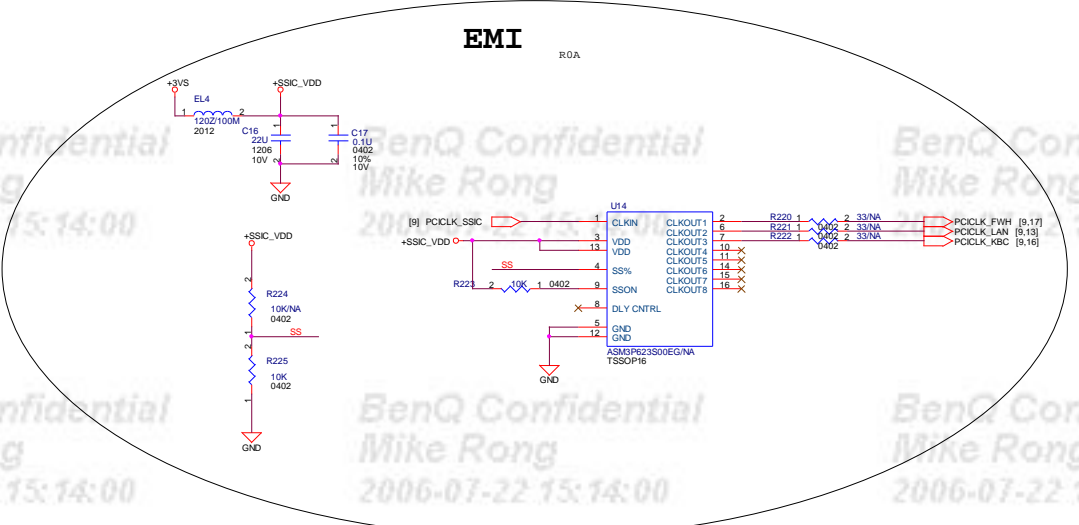
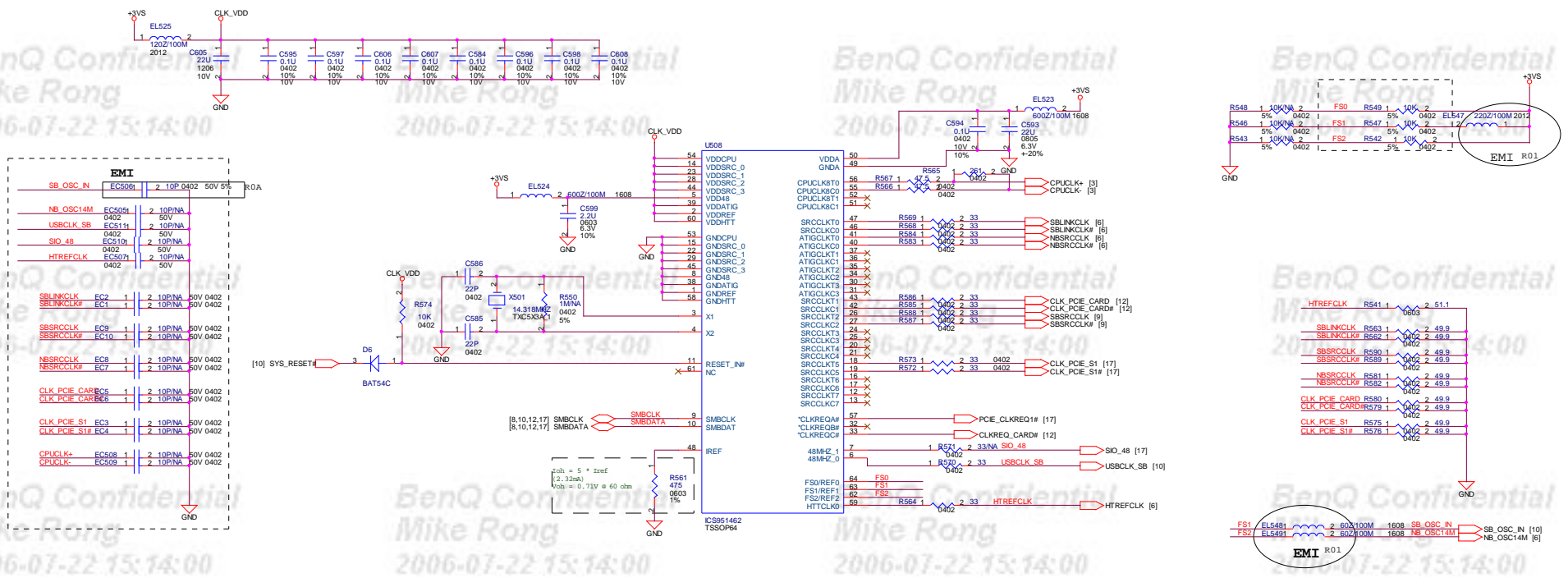
CPU-K8 Dual Core (2/2)



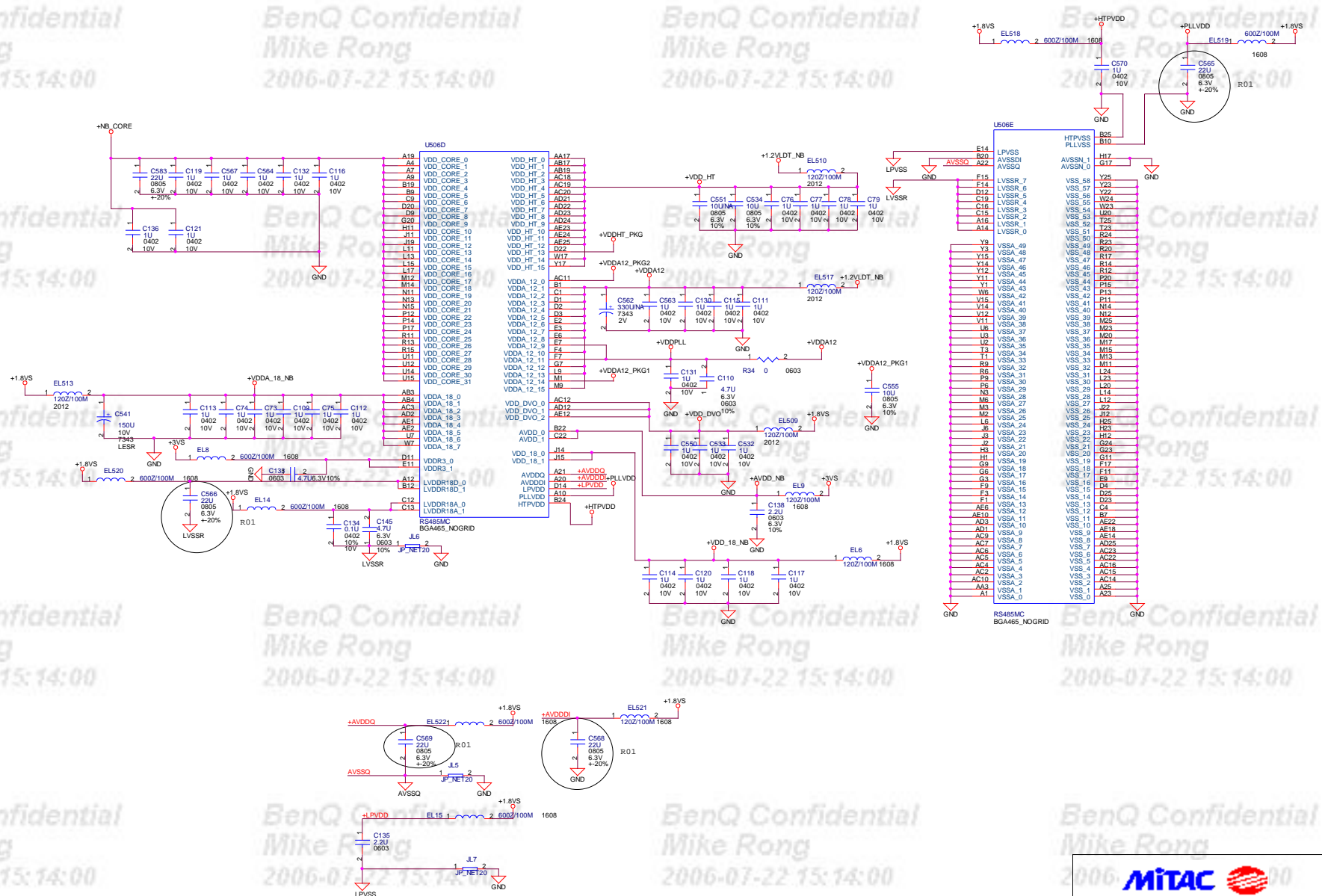
MITAC logo

Title	K8 Dual Core(1/2)				
Size	Document	ASSY/PCB 41180810001/31680810001	Rev	R02	
Date	Thursday, May 04, 2006	Sheet	4	of	27

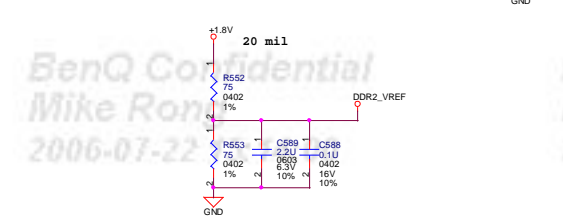
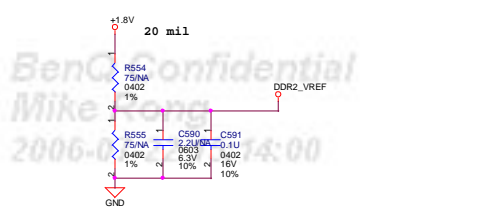
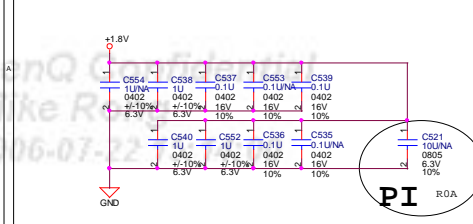
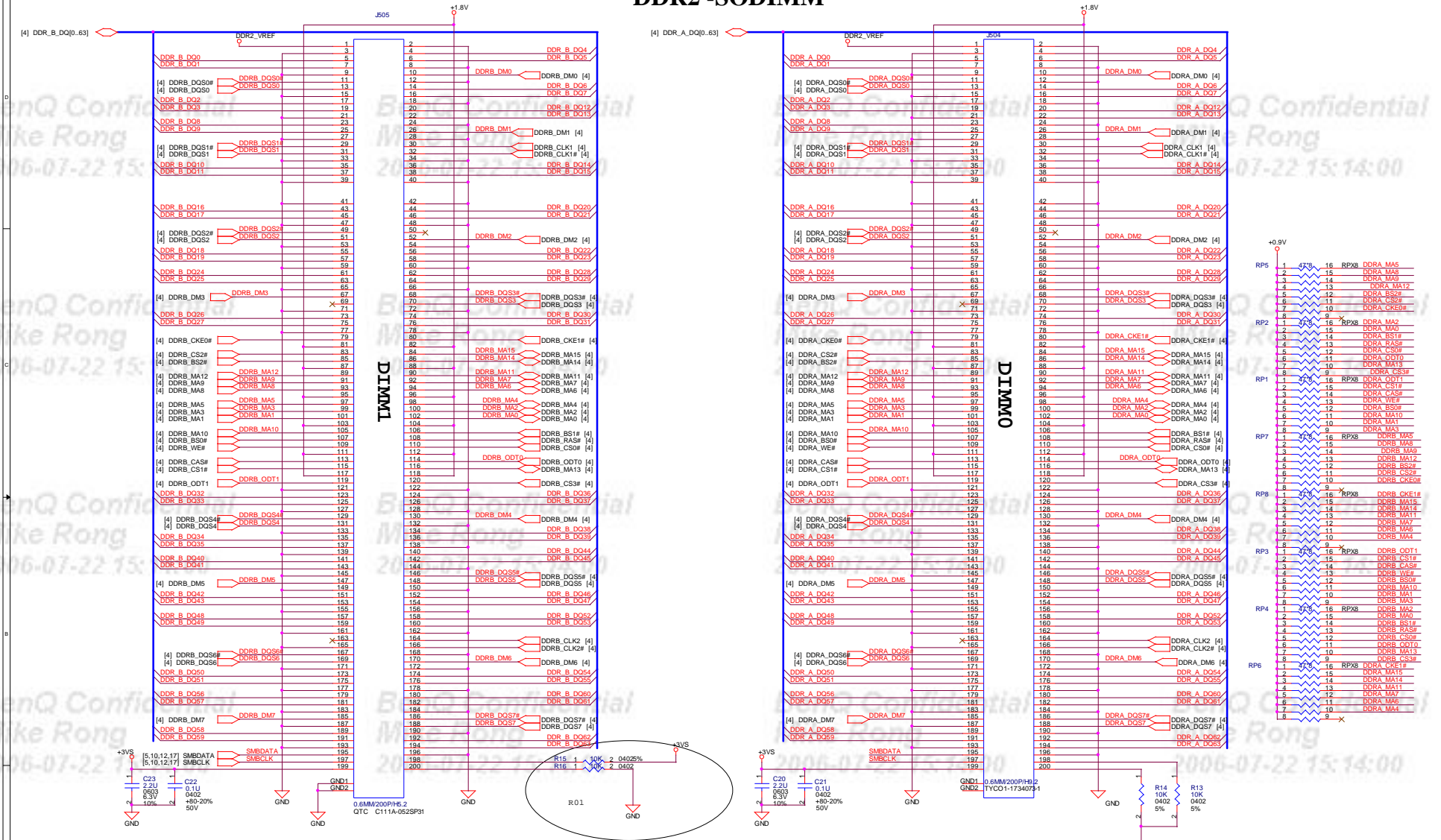
CLOCK GEN ICS951462



NB - ATI RS485 (2/2)

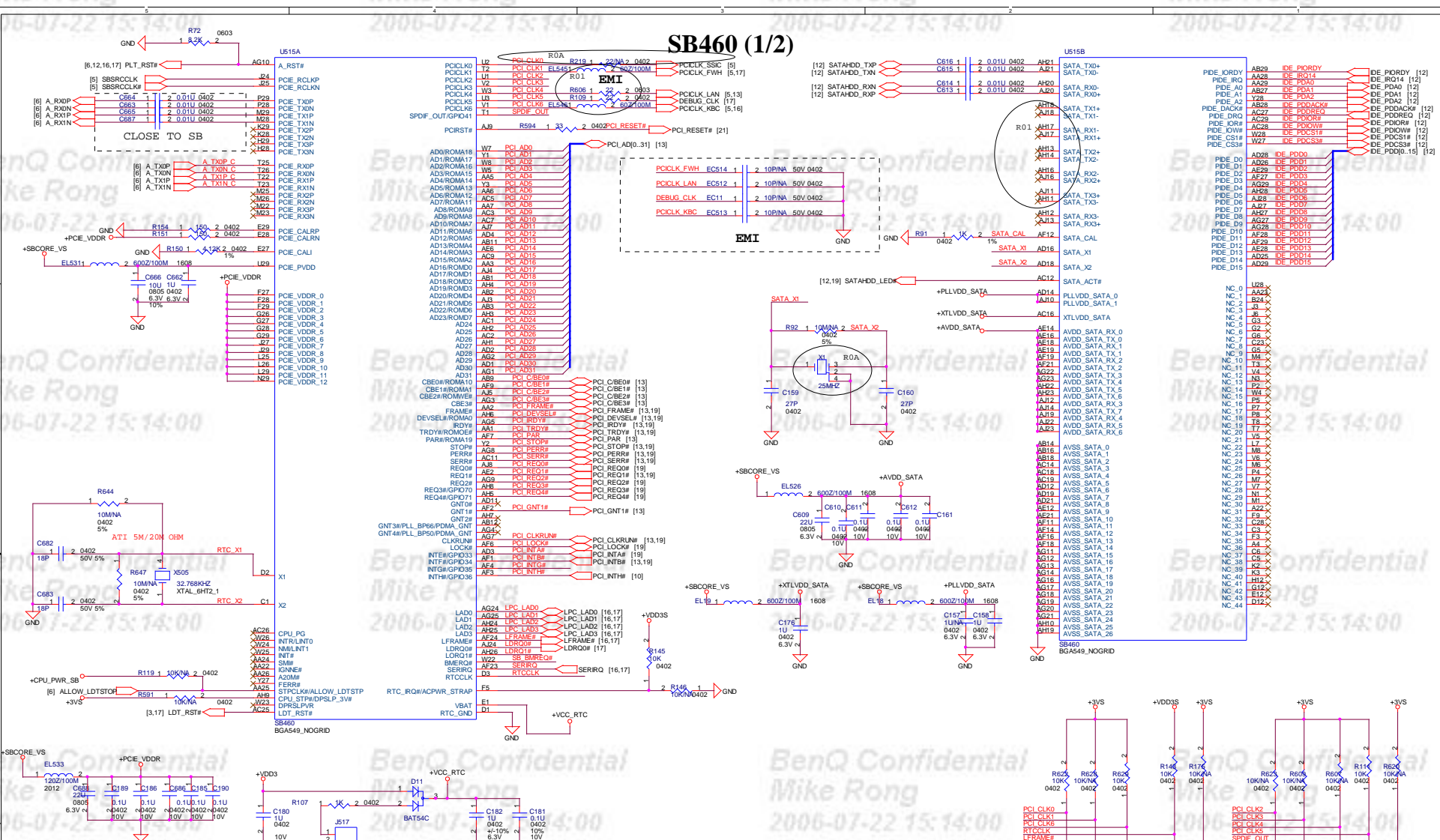


DDR2 -SODIMM

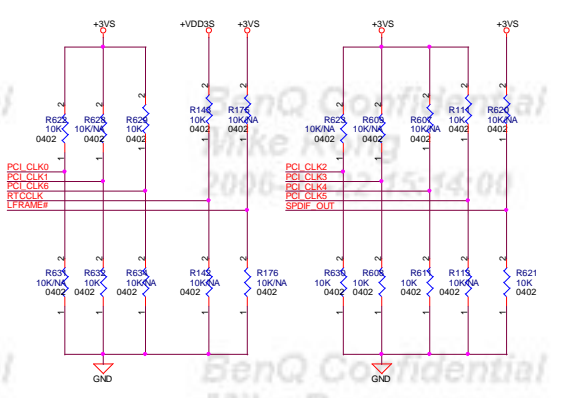


Title	DDR2 SODIMM		
Size	C	Document Number	ASSY/PCB 41180810001/31680810001
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SB460 (1/2)



	HIGH	LOW
RTC_IRQ#	Manual power on (default)	Automatic power on
AC_SDOUT	Enable debug straps	Disable debug straps (Default)
RTCCLK	Enable internal RTC (Default)	Enable external RTC
SPDIF_OUT	24MHz SIO_CLK	48MHz SIO_CLK
PCI_CLK2	48MHz XTAL mode	48MHz OSC/CLK Buffer mode (Default)
PCI_CLK3	Disable USB Phy power down	Enable USB Phy power down (Default)
PCI_CLK4	Use internal USB PLL	External USB 48MHz source (Default)
PCI_CLK5	PCIE lane auto detect (Default)	Force to 2PCIE lanes
PCI_CLK6	X8 cpu interface (Default)	P4 cpu interface
LFRAME#	Enable THERMTRIP# on power up	Disable THERMTRIP# (Default)



MITAC

File: SB-SB460(1/2)

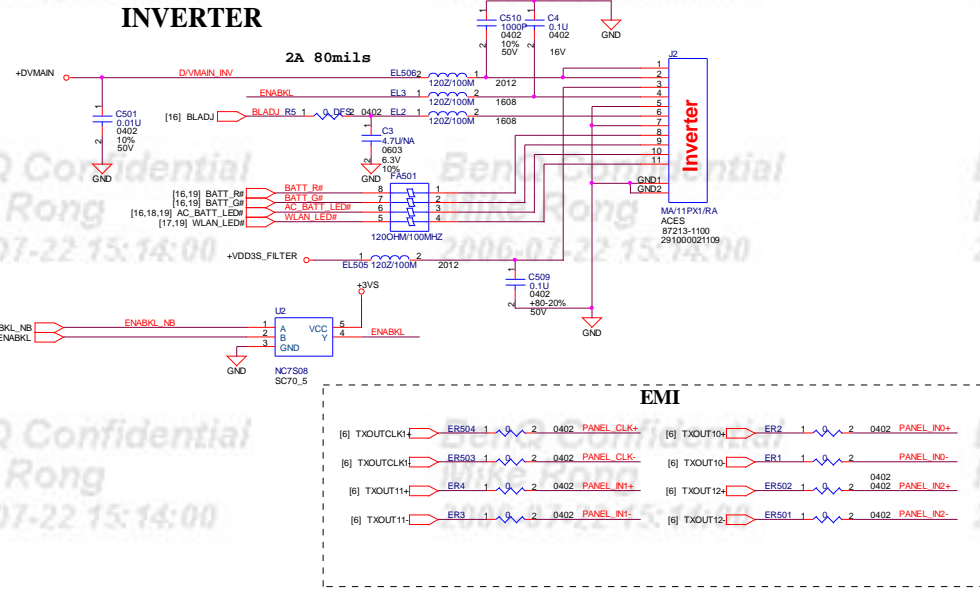
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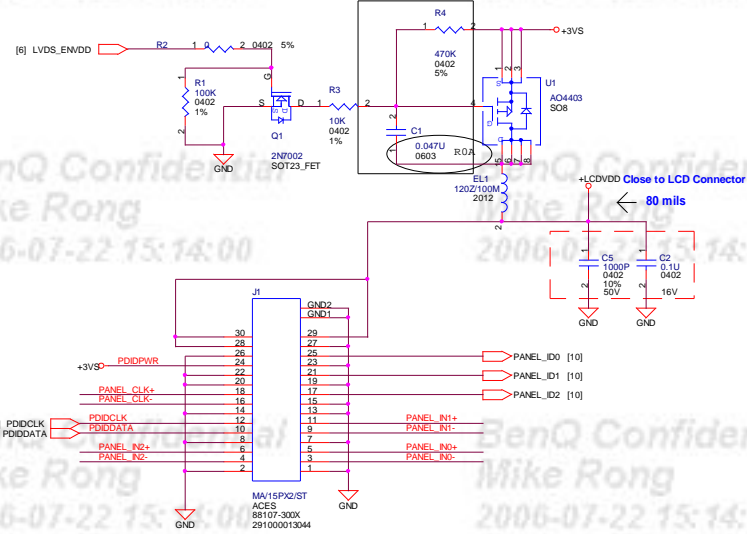
Date: Thursday, May 04, 2006

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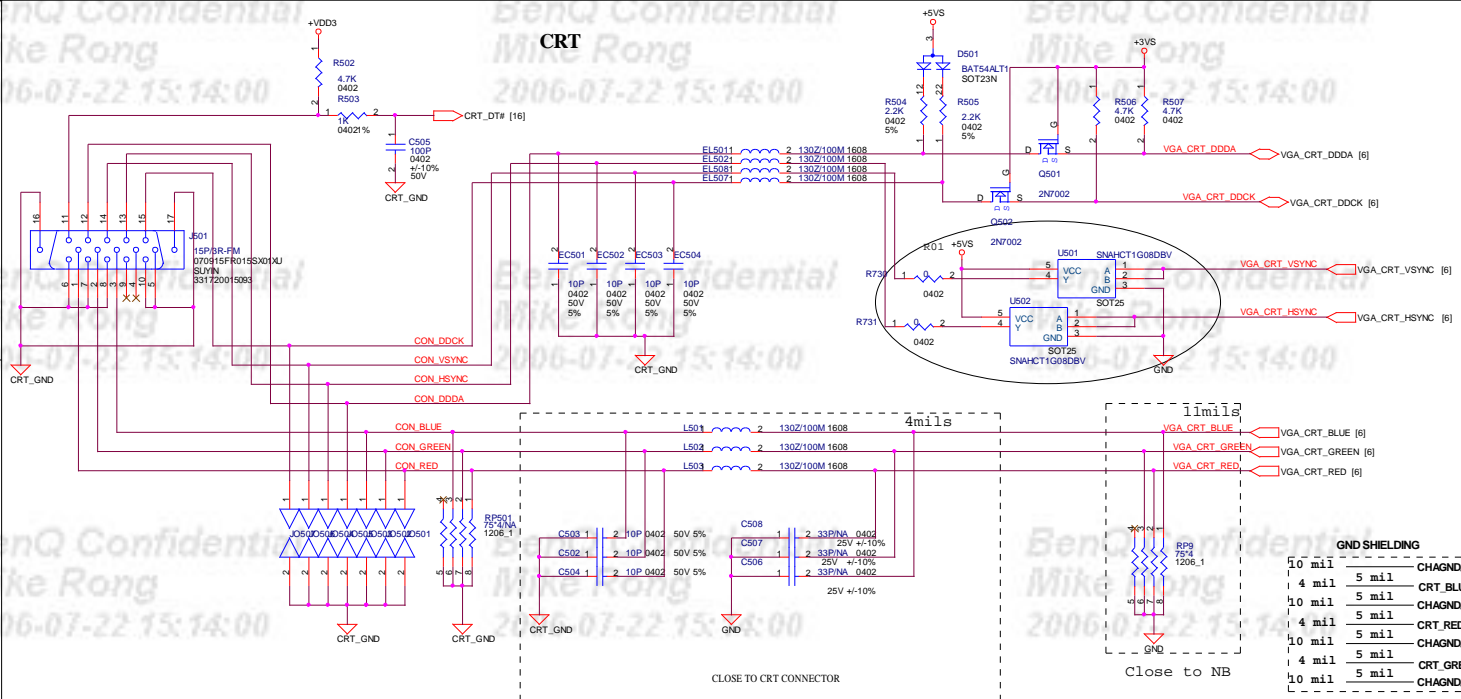
INVERTER



LCD



CRT



GND SHIELDING

10 mil	CHAGND/GND
4 mil	CRT BLUE
10 mil	5 mil CHAGND/GND
4 mil	CRT RED
10 mil	5 mil CHAGND/GND
4 mil	CRT GREEN
10 mil	5 mil CHAGND/GND

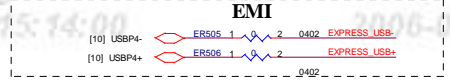
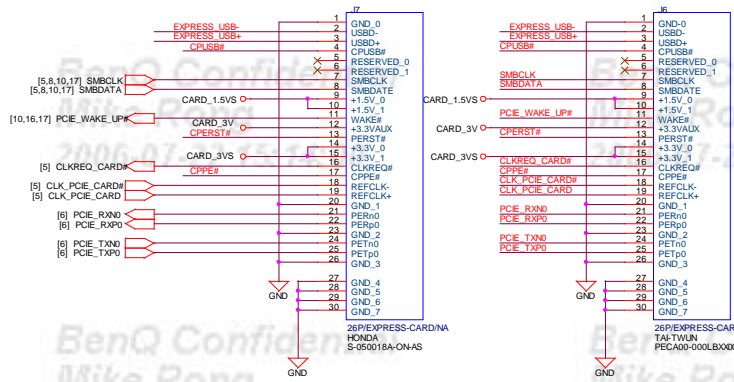
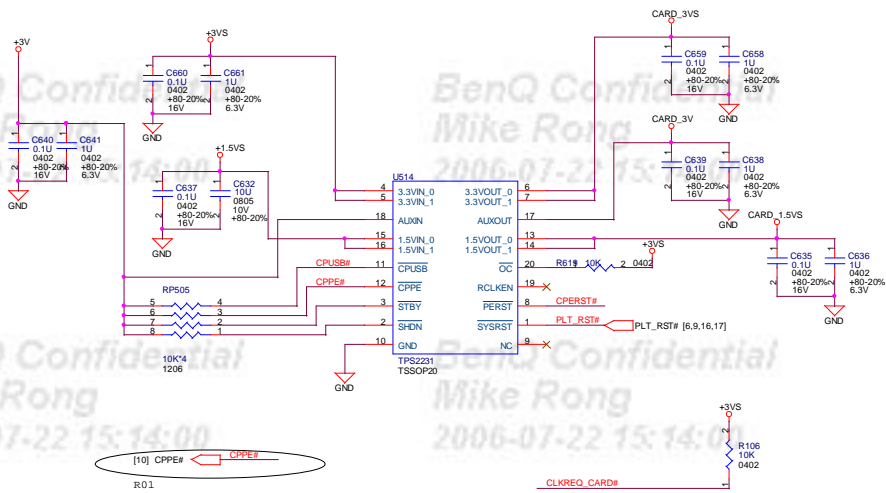
MITAC

File: Display CRT/LCD

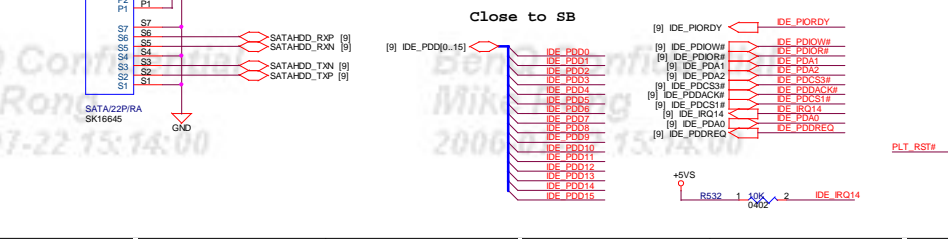
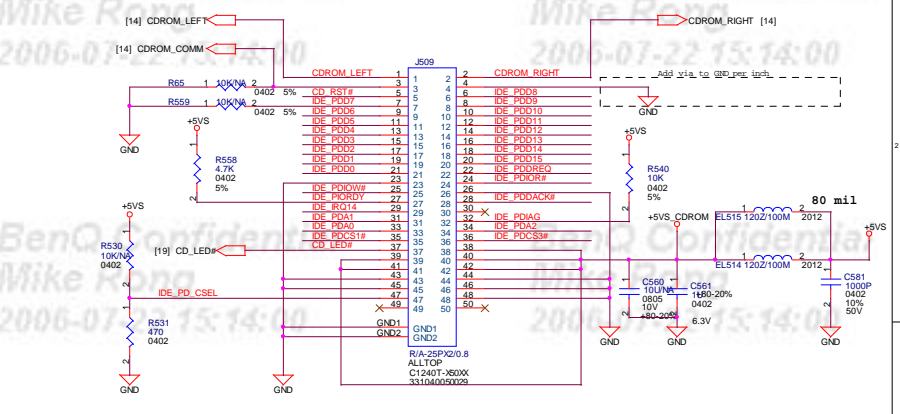
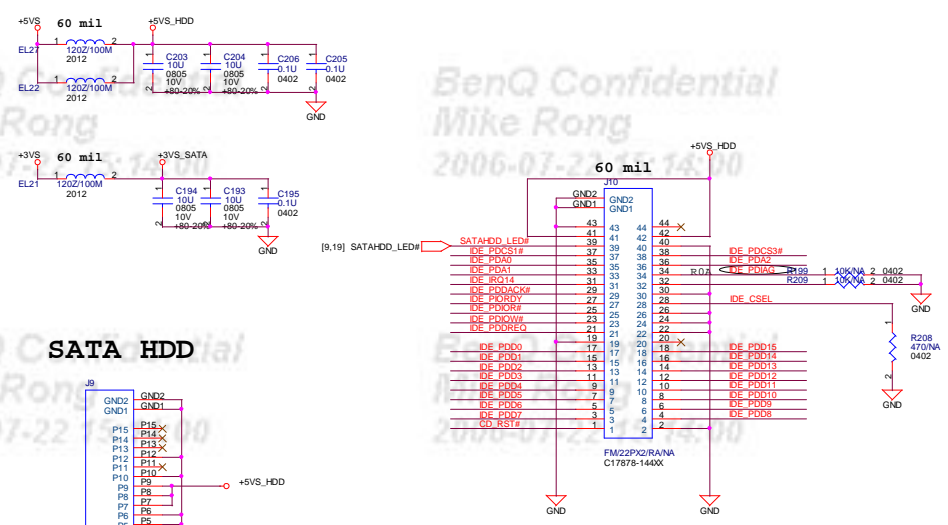
Size: Document ASSY/PCB 41180810001/31680810001 Rev: R02

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SATA / IDE/Express Card



IDE CD-ROM CONNECTOR

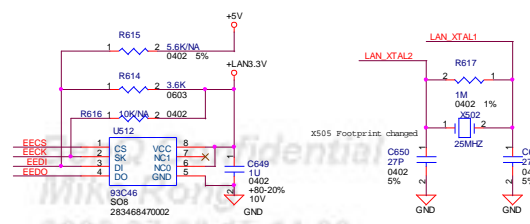
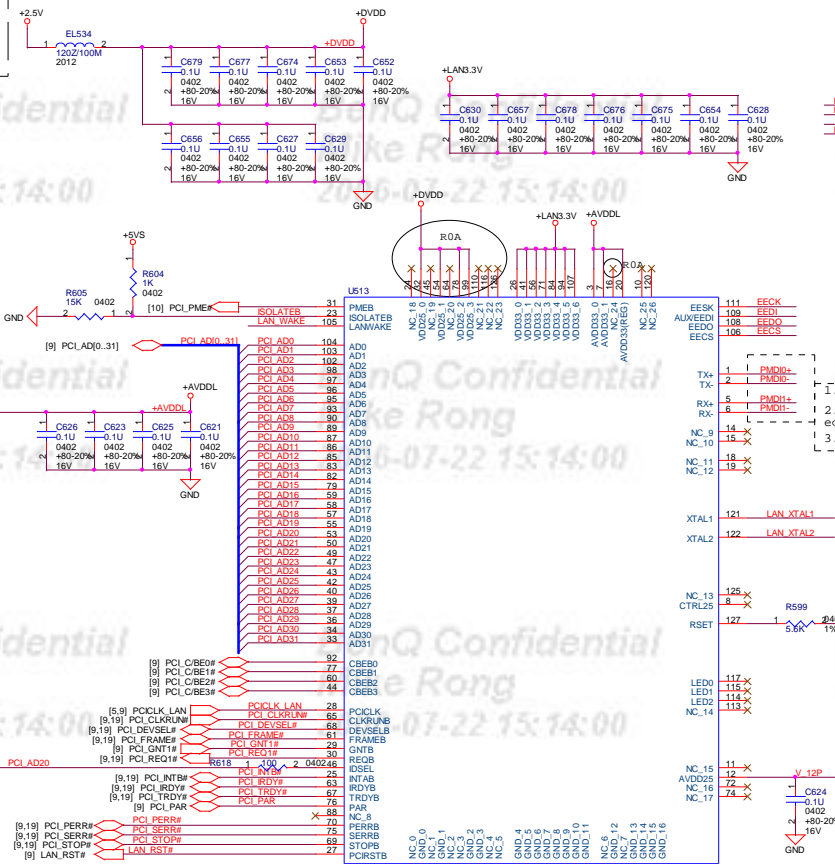


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Size	C	Document Number	ASSV/PCB 41180810001/31680810001
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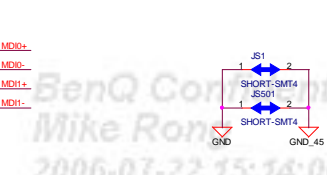
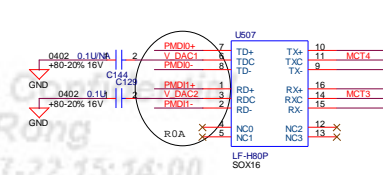
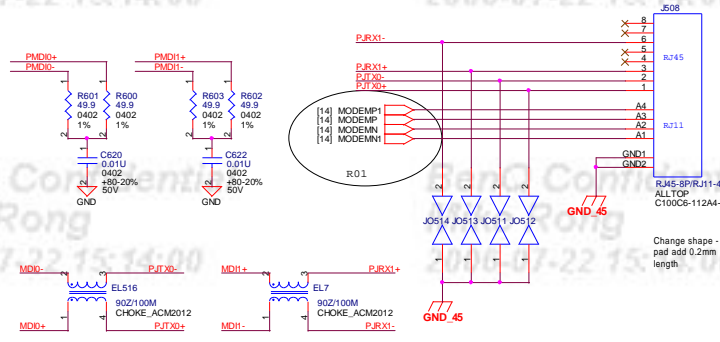
LAN-RTL8100CL

RTL8100CBL

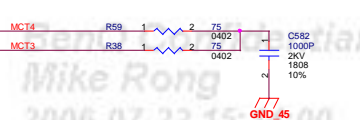
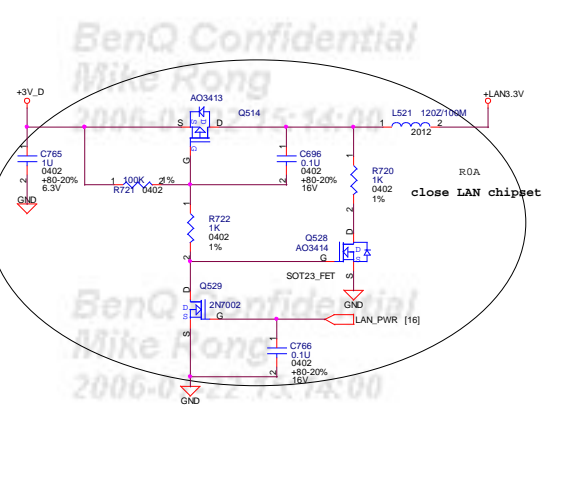
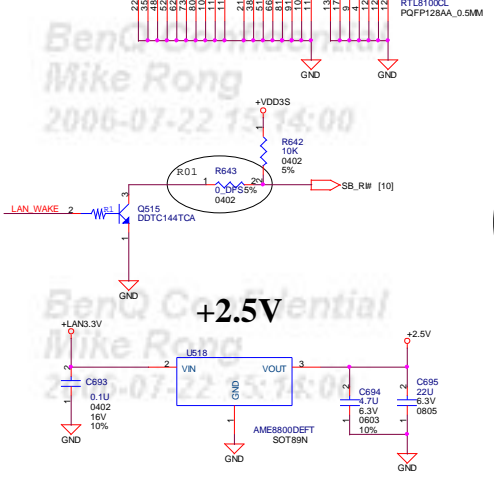
AD20
PCL_INTB#
REQ1#/GNT1#



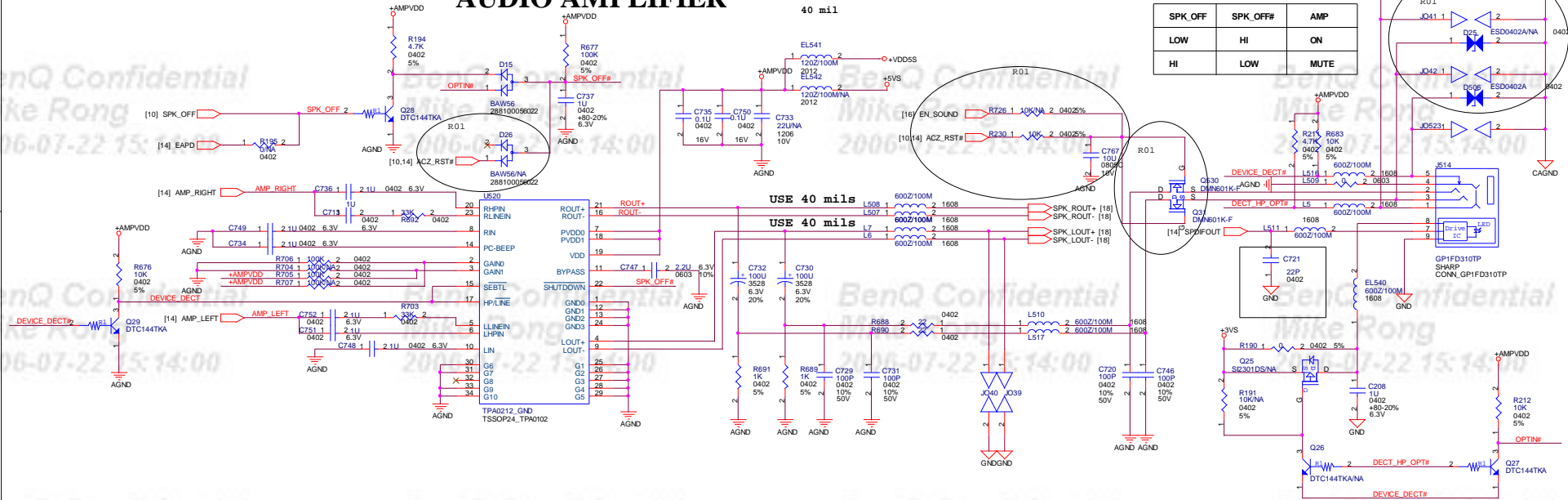
Crystal should be placed far away from I/O port and Tx,Rx,power,magnetics.



Signal	Value
AVDDH	N/A
V_12P	+2.5V
AVDDL	+3V
V_DAC	N/A
DVDD	+2.5V
DVDD_A	N/A



AUDIO AMPLIFIER

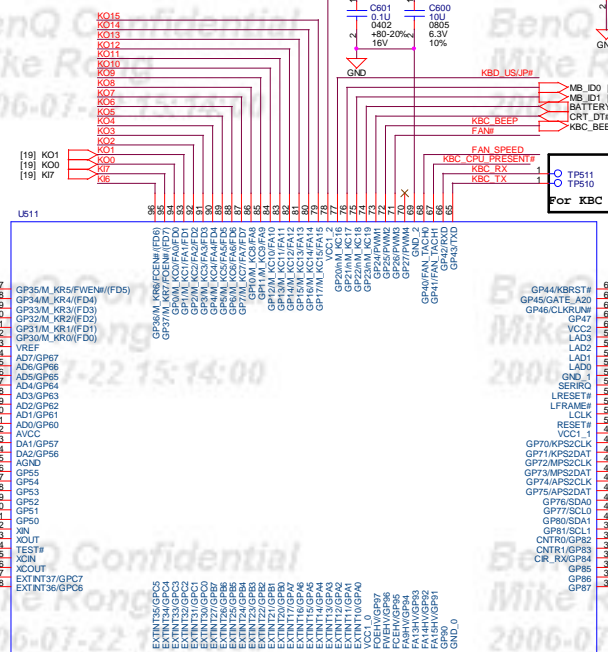
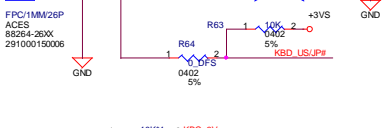
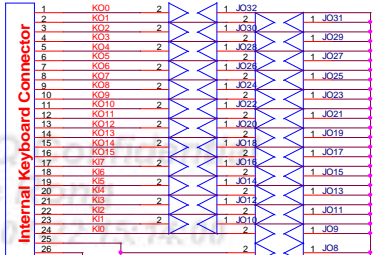


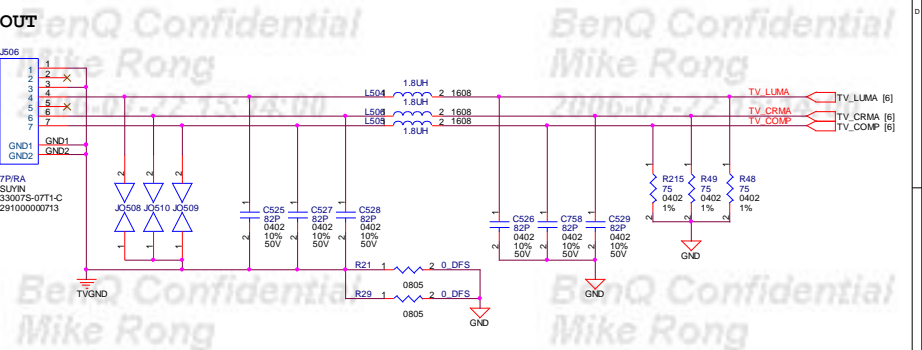
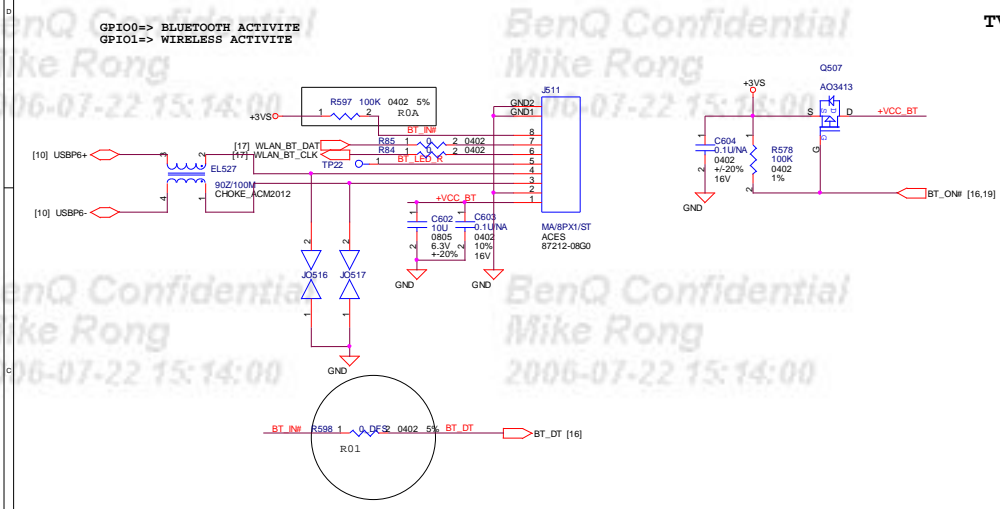
SPK_OFF	SPK_OFF#	AMP
LOW	HI	ON
HI	LOW	MUTE

MITAC

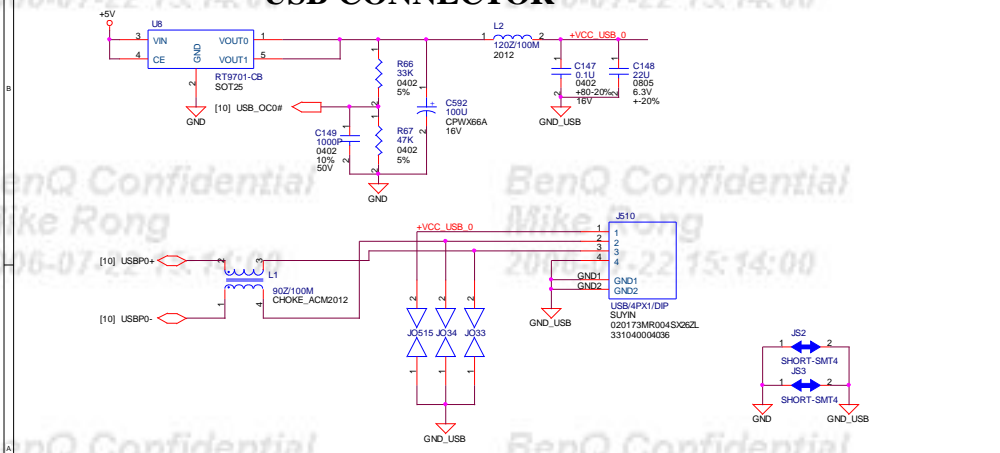
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Size C	Document Number ASSY/PCB 411808100001/316808100001	Rev R02
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WINBOND KBC

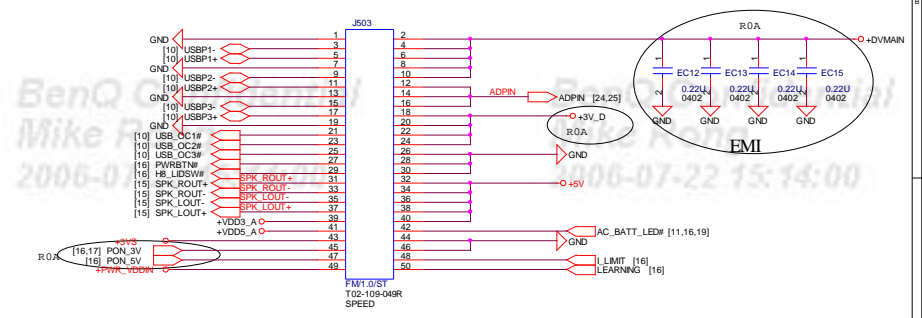




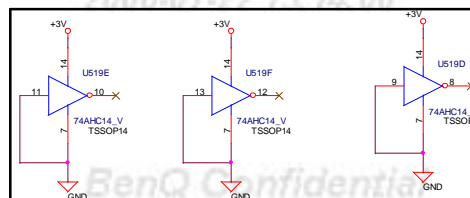
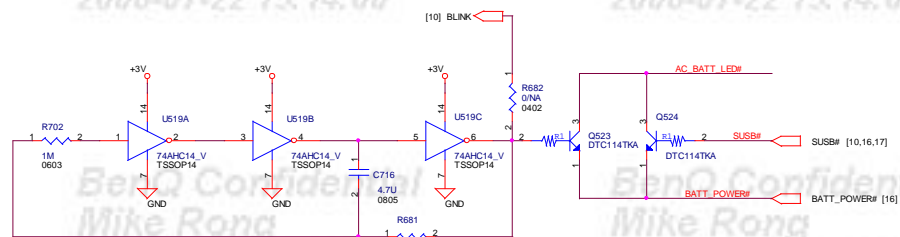
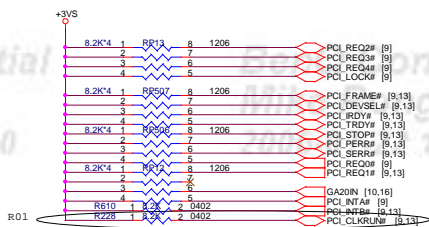
USB CONNECTOR



BOARD TO BOARD CNN



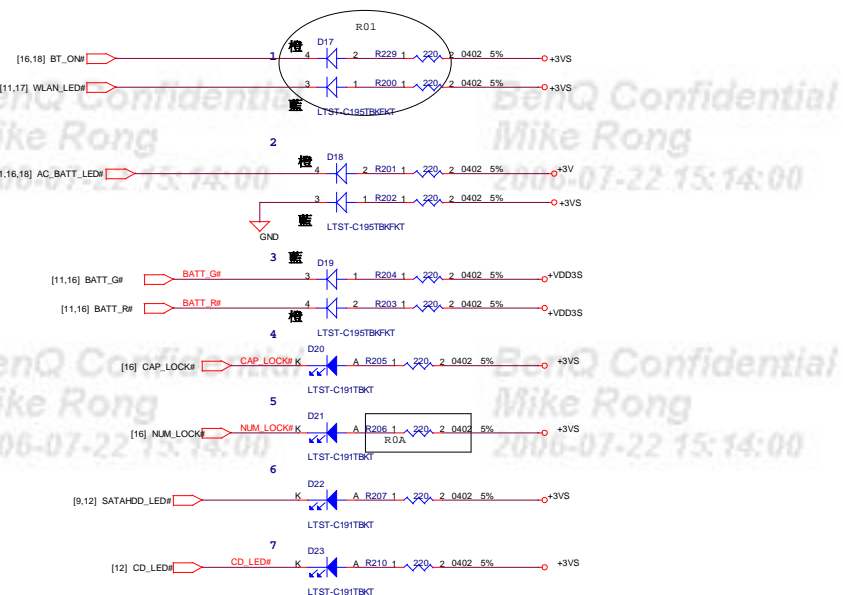
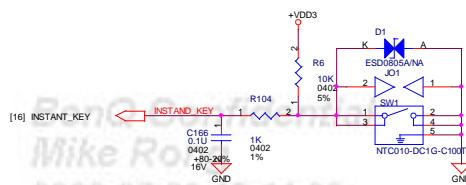
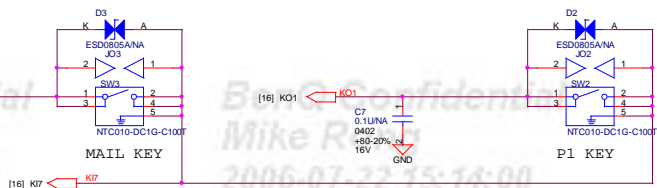
PCI PULL HIGH



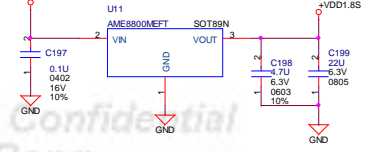
LED

LED

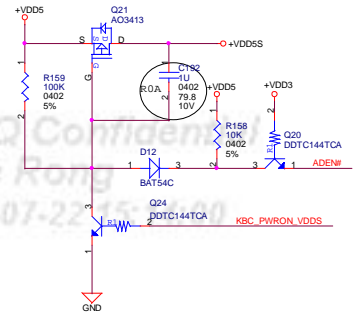
LED	1	2	3	4	5	6	7
	WLAN/BT	AC/Battery	Charger	Caps Lock	Num Lock	HDD	ODD



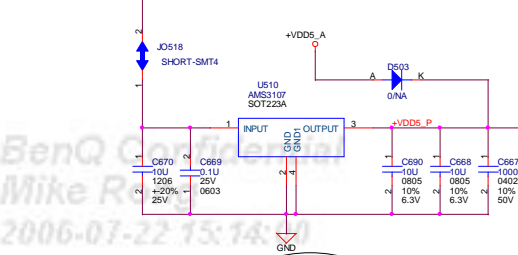
+VDD1.8S



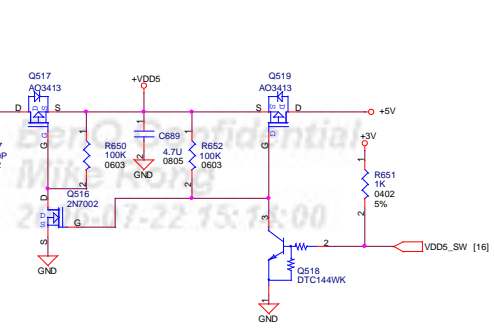
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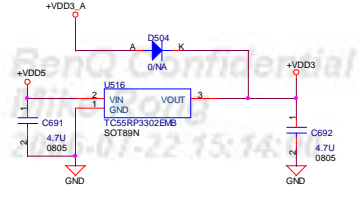
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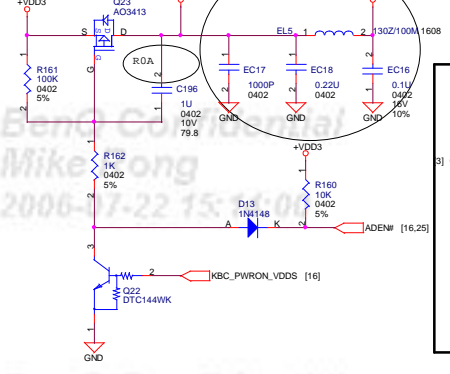
PERIPHERIAL



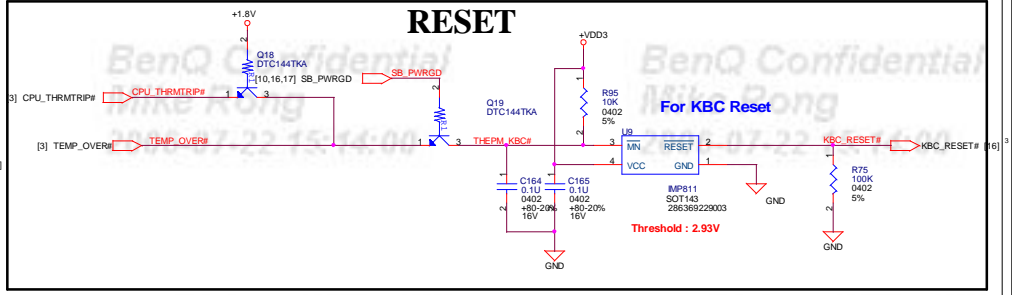
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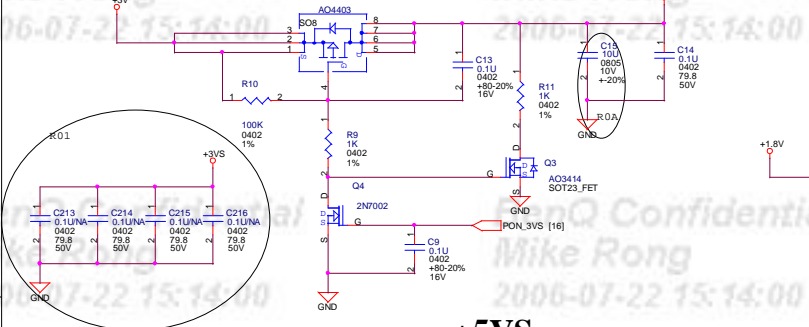
+VDD3S



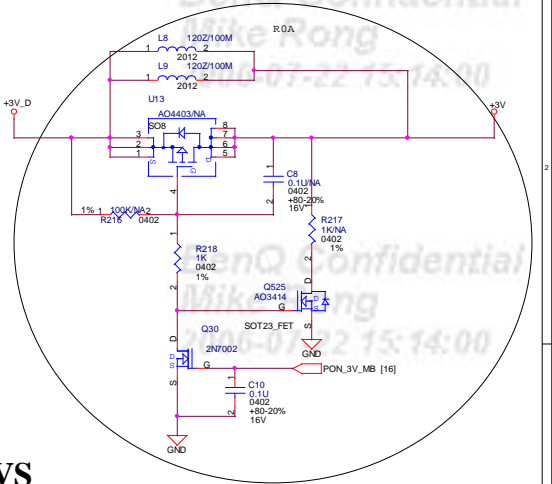
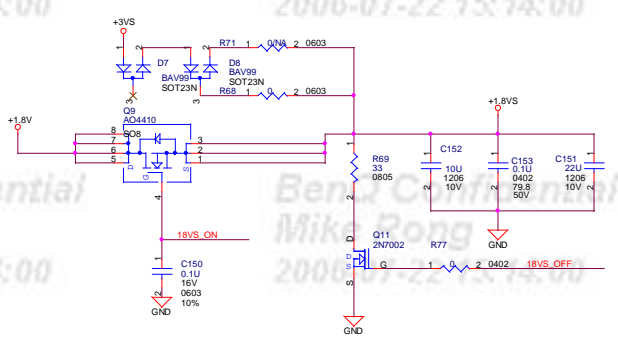
RESET



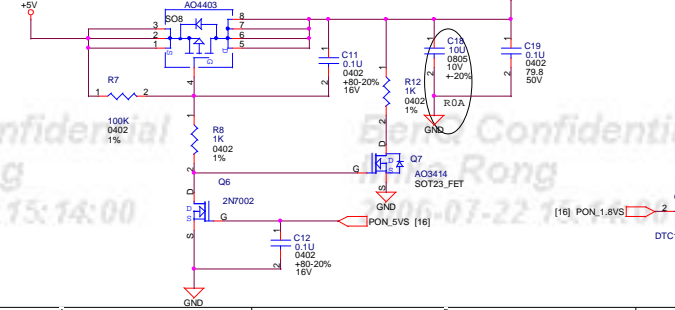
+3VS



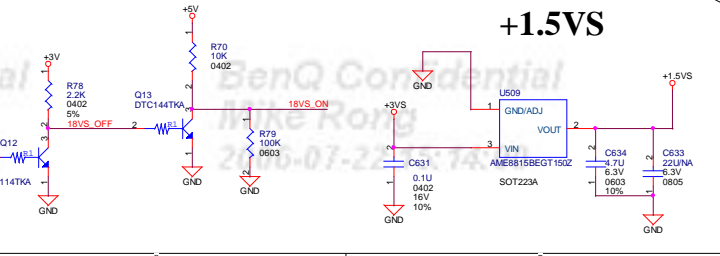
+1.8VS



+5VS

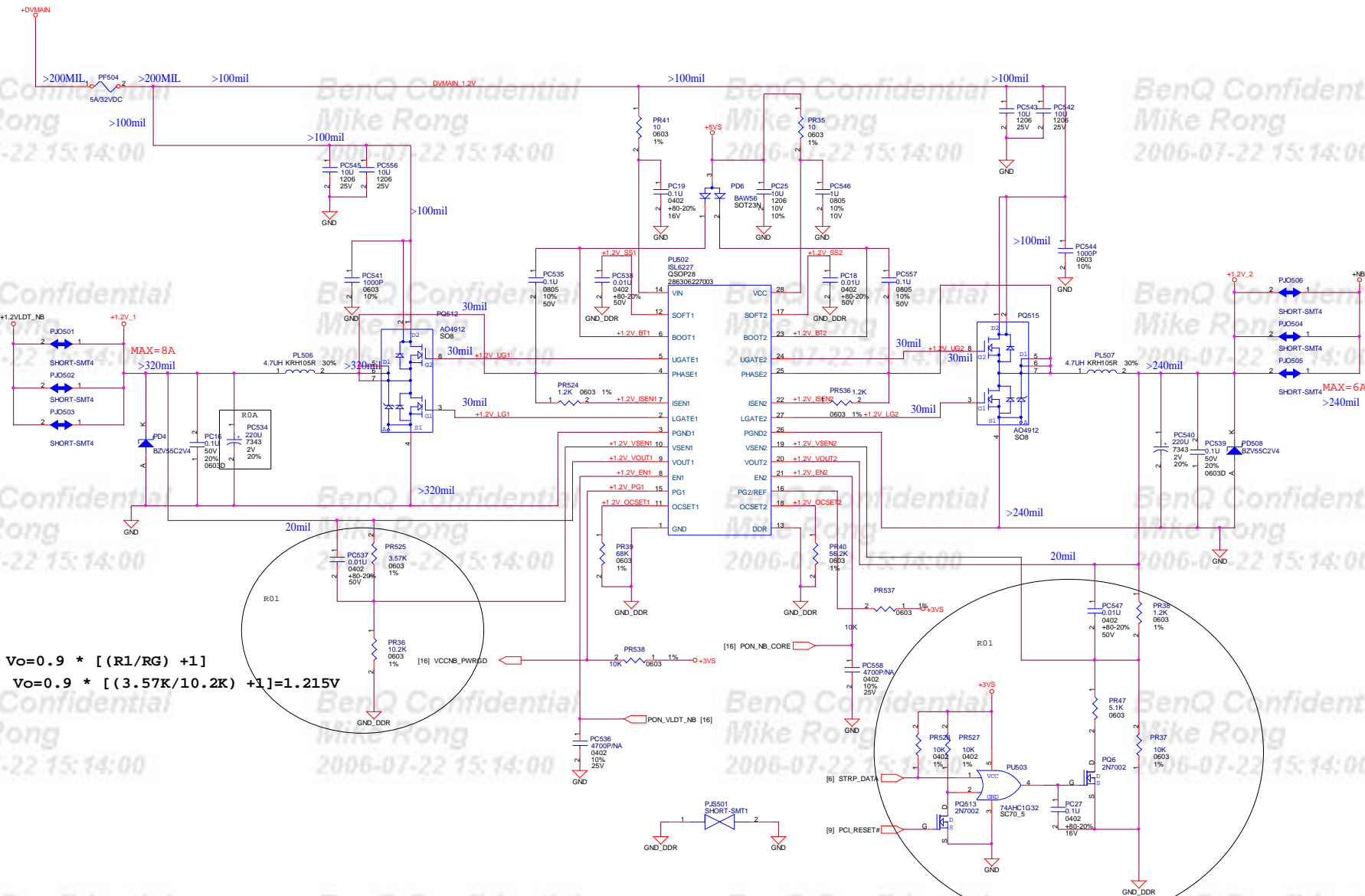


+1.5VS



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+1.2V_P1 / +1.2V_P2



$$V_o = 0.9 * [(R1/RG) + 1]$$

$$V_o = 0.9 * [(3.57K/10.2K) + 1] = 1.215V$$

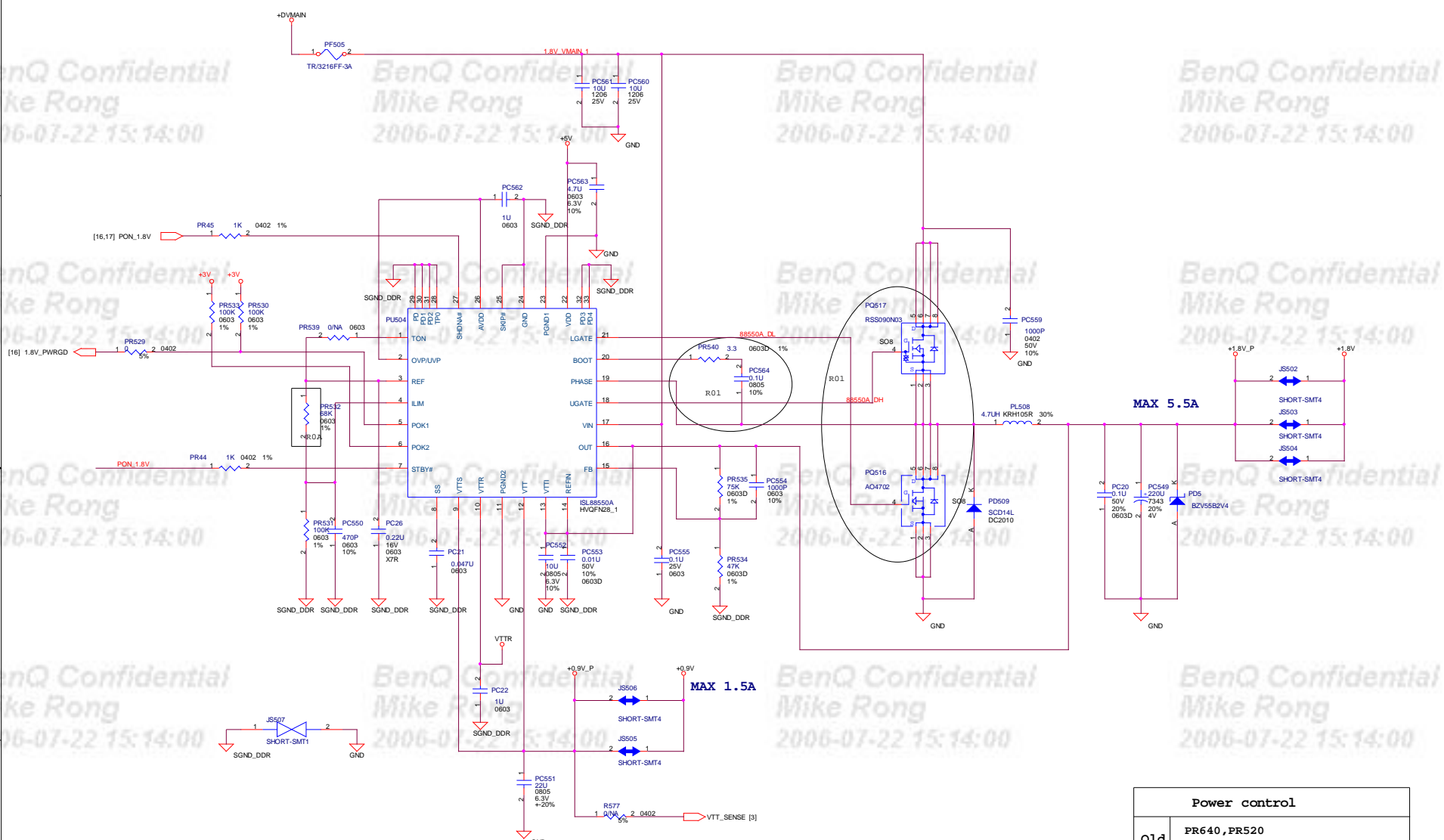
$$V_o = 0.9 * [(R1/RG) + 1]$$

$$V_o = 0.9 * [(1.2k/10K) + 1] = 1.008V$$

$$V_o = 0.9 * [(1.2k/(10K/5.1K)) + 1] = 1.21976V$$

Title	+1.2V_P1 / +1.2V_P2	
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DDR2 +1.8V_P/+0.9V_P

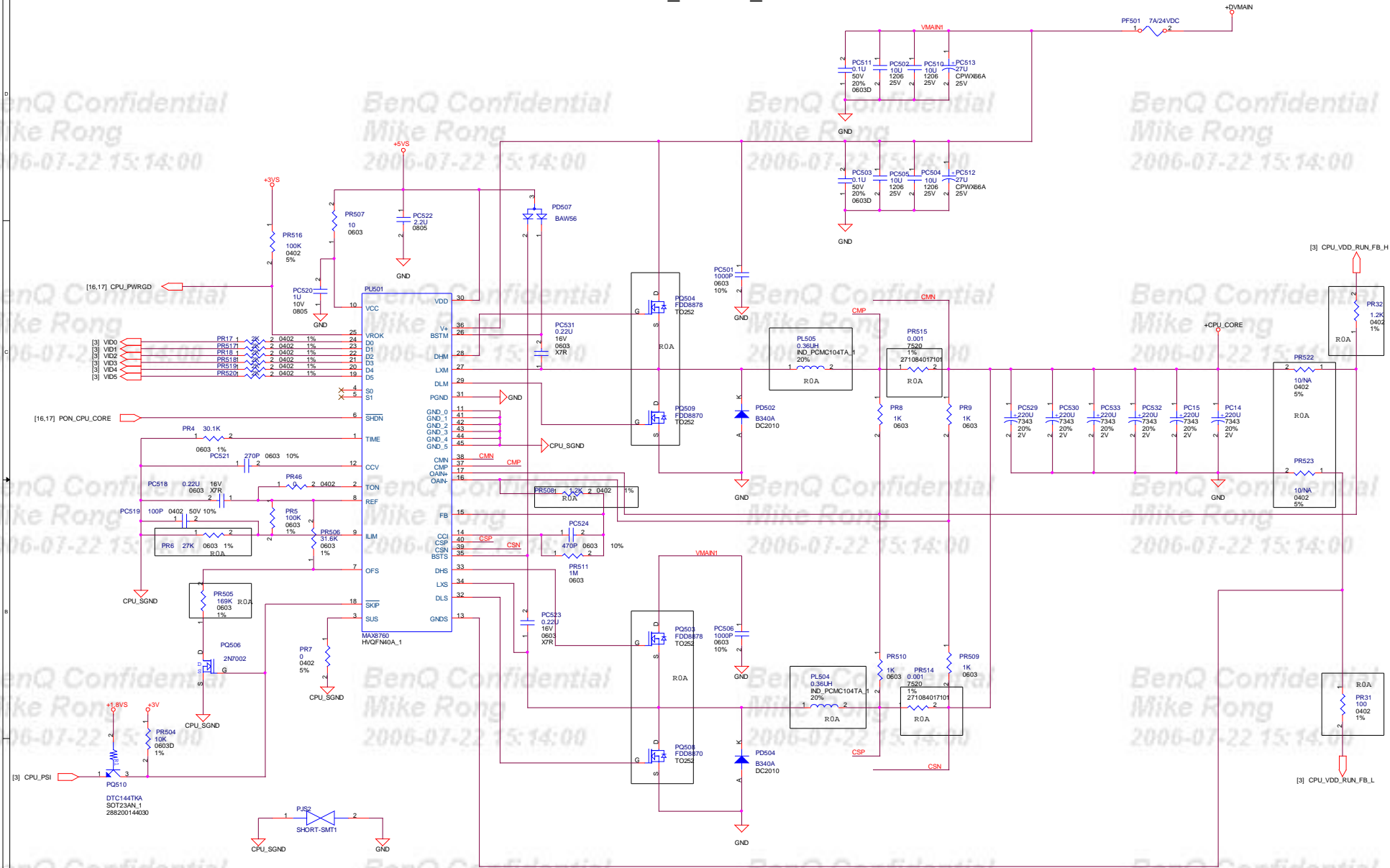


Power control	
Old	PR640, PR520
New	PR673, PR674, PR642, PR512

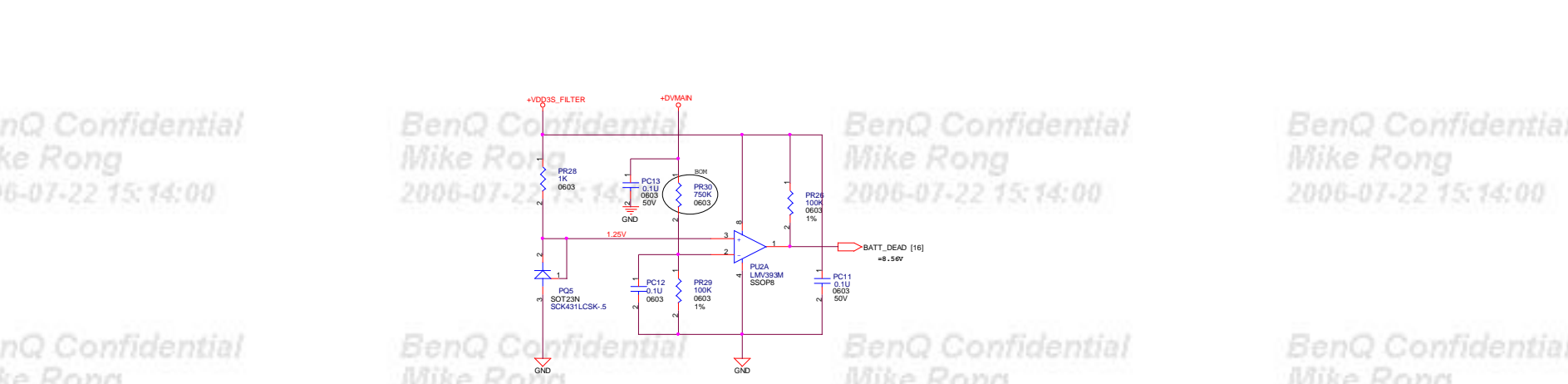
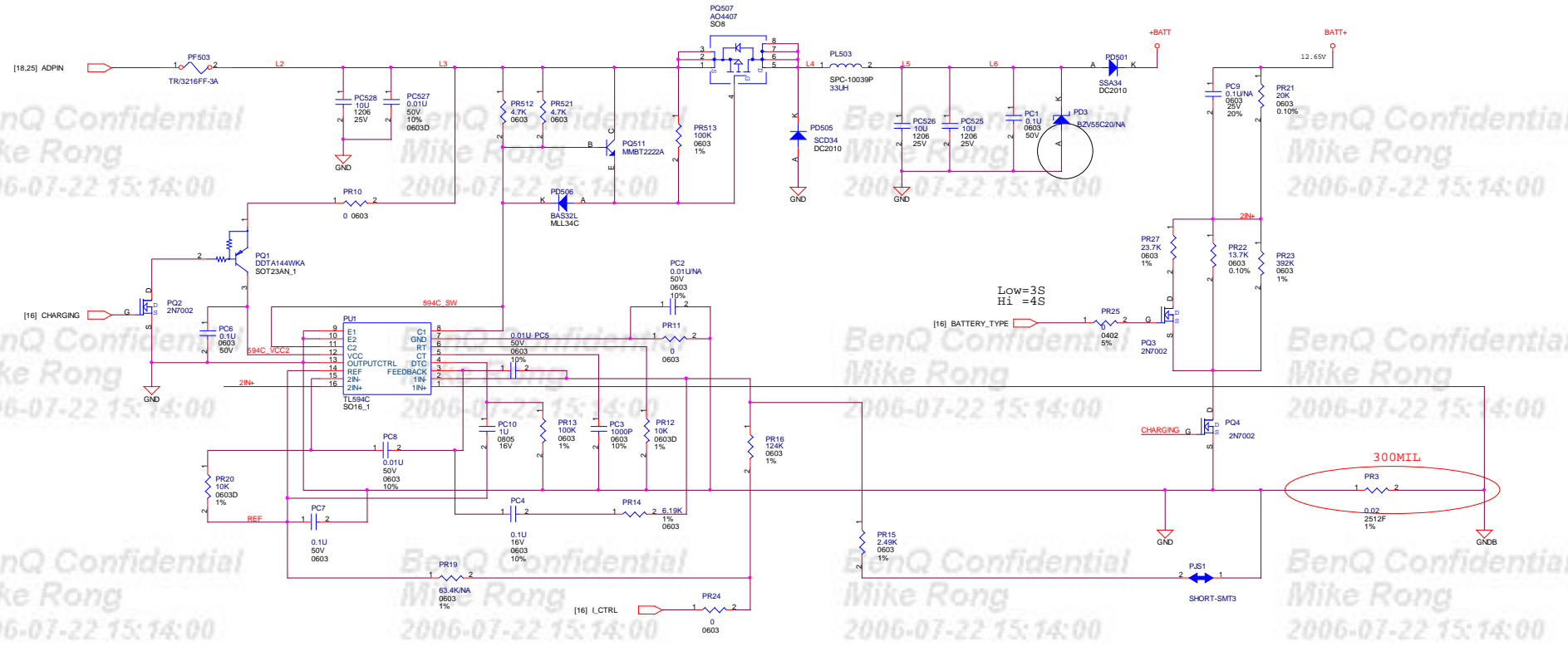
MITAC

Title	+1.8V_P/+0.9V_P(ISL88550A)	
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CPU_CORE_MAX8760



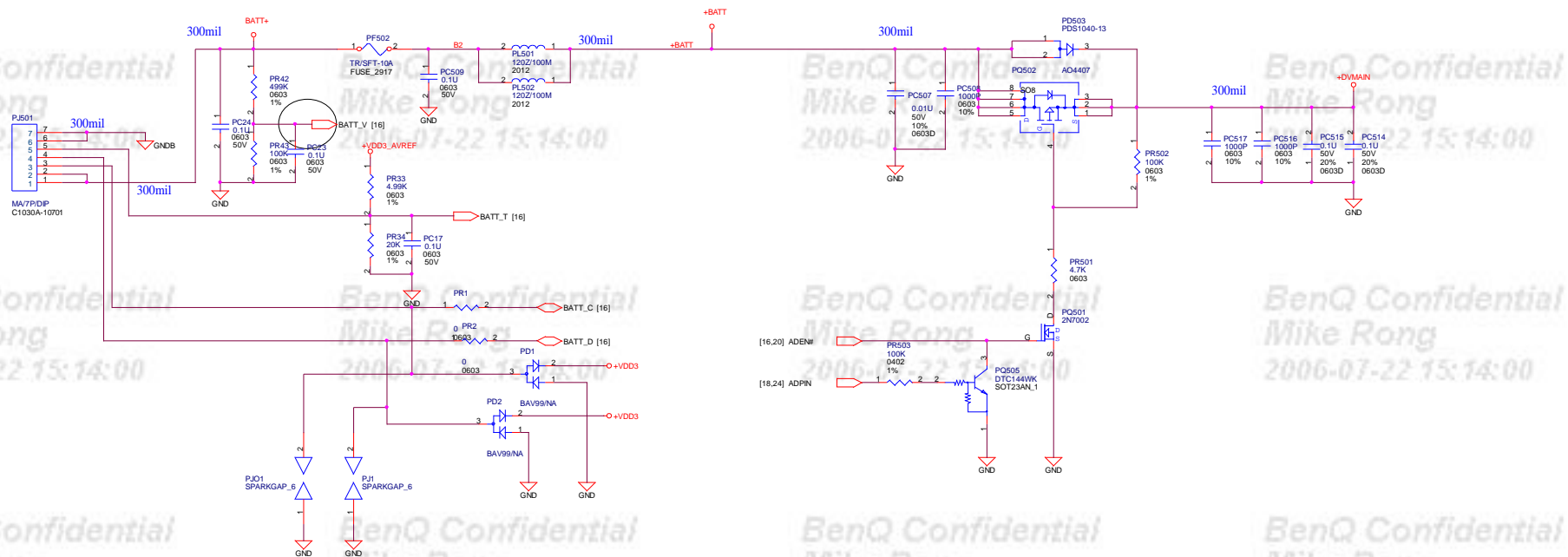
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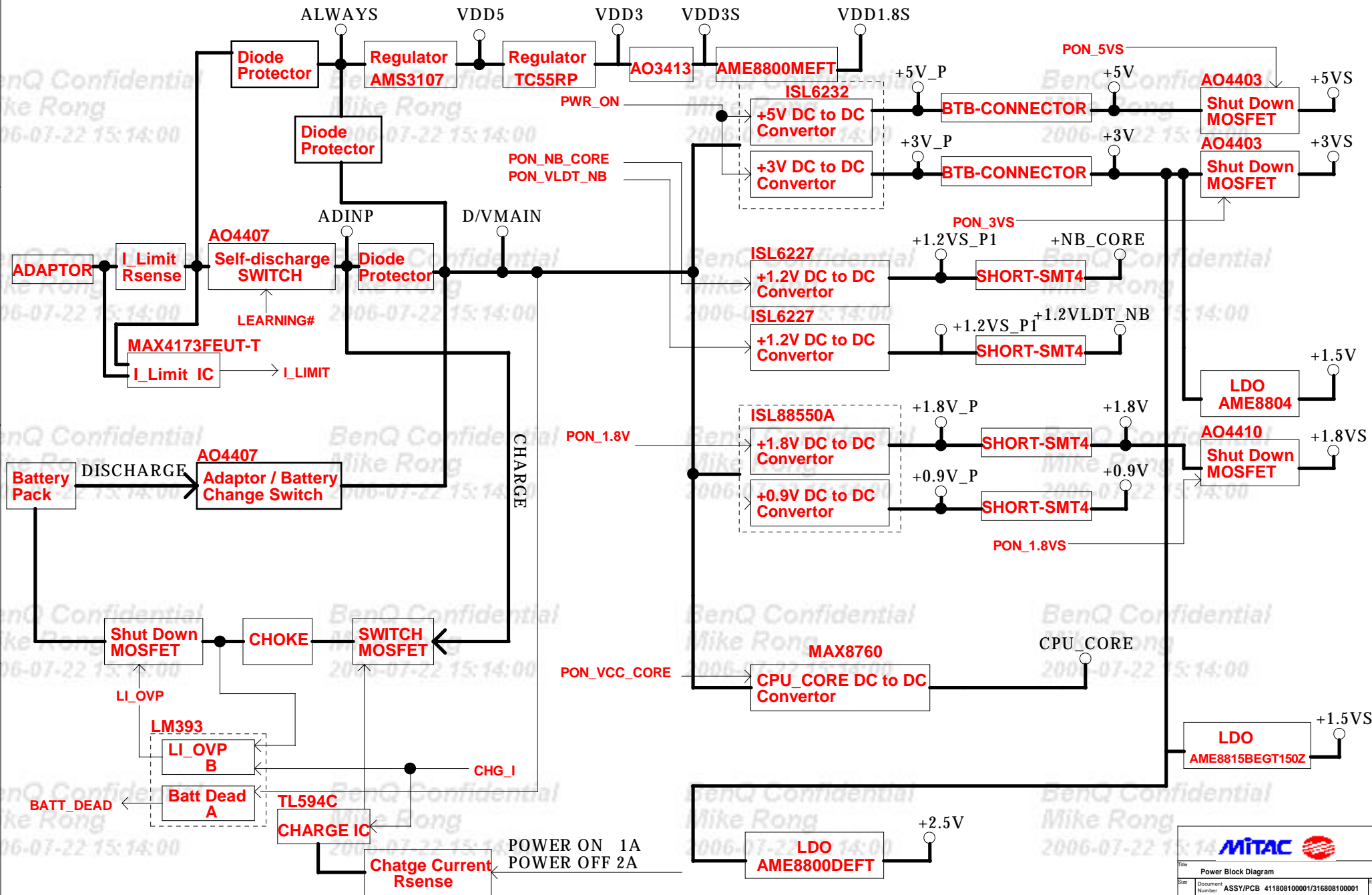
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DISCHARGE



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POWER BLOCK DIAGRAM



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REVISION	TAPEOUT DAY	PAGE	HISTORY
R01	2006.04.11		(1)Change EL10 to 0805 package. (2)Change R544,R545 to EL548,EL549 bead for EMI. (3)Add EL547 for EMI. (4)Change C565,C566,C568,C569 to 22uF 0805 for projector issue. (5)Add TP29,TP30,TP31 for EMI. (6)Change R15 pull high,R16 pull low to correct RAM setting. (7)Change R624,R626 to EL545,EL546;R606 to 0603 package for EMI. (8)Remove SATA TX pull low for ATI recommend. (9)Add R724 for KB_RST# damping. (10)Add CPPE# to SB GPIO for NEW CARD hot plug. (11)Add R730,R731, change U501,U502 to 5V level for projector issue. (12)Correct MODEM pin connection. (13)Change R710,R712 to 10k ohm for "bo" sound issue. (14)Add R230,R726,C767,Q530,Q31,D26 for "bo" sound issue. (15)Change D24,D506 to TVS for ESD. (16)Add R728,U523,C772 for RSMRST# timing request. (17)Change Q510,Q511 to 2N7002 for auto restart when AC/Battery mode swap. (18)Add EN_SOUND from KBC for "bo" sound issue. (19)Change R82,R635 to bead. (20)Add R229 and change D17 to dual-led for BT display. (21)Add EL5,EC16,EC17,EC18 for EMI. (22)C213,C214,C215,C216 for +3VS to GND decouple. (23)change STRP_DATA and relative circuit to support powerplay. (24)Add PR540, change PQ516 to RSS090N03, PQ517 to AQ4702 for 1.8V switching noise.

R02	2006.05.04		(1)Connect U515.T2 and EL545.1 to PCI_CLK1 to correct PVT lost.
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